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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,065	12/29/2003	Oceager P. Yee	Yee 6	8310

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,065	YEE, OCEAGER P.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Dec 29, 03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 3 recites the limitation "said configuring" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Moberly (U.S. Patent number 6484280).

3. As per claim 1, Moberly teaches (col. 2, lines 52-55) a system-on-a-chip (SOC) to which scan path has been added. He also teaches that each of the functional blocks is isolated for test by scan path wrappers. He thus teaches an SOC having at least one functional block, controlled by a block clock and at least one scan chain. He also teaches (col. 2, lines 59-62) that a specific scan chain may be selected by chain selector which is controlled by test access port. He thus teaches limitations pertain to debug trigger signal, selecting from the at least one scan chain containing at least one register element. He further teaches (col. 3, lines 5-7) a control signal TMS gates input signal through multiplexer, a test clock TCK that shifts the inputs present at serial input line and

outputs are shifted out serial output line TDO. He thus teaches providing control of the selected scan chain, shifting out the contents of the at least one register element in the selected scan chain and utilizing contents to debug the SOC.

4. As per claim 2, With reference to recognizing a debug ack signal inputted by a user. Moberly teaches (col. 3, lines 5-7, lines 59-61).

5. As per claim 3, With reference to identify a subsequent scan chain, repeating the configuring, providing, shifting and utilizing steps. Moberly teaches (col. 4, lines 13-17).

6. As per claim 4, With reference to recognizing the deactivation of the debug signal and returning each block clock to its operative state. Moberly teaches (col. 3, lines 12-15).

7. As per claim 5, With reference to configuring each of the at least one register elements in the selected scan chain with test values. Moberly teaches (col. 4, lines 1-5).

8. As per claim 6, With reference to disabling all clocks to the cells containing nonscan flip-flops and disabling all clocks to the cells while the debug trigger signal is active. Moberly teaches (col. 3, lines 18-20).

9. As per claim 7, With reference to controlling a bidirectional data bus, and disabling the devices while the debug trigger signal is active. Moberly teaches (col. 3, lines 17-20, 40-43).

10. As per claim 8, Moberly substantially teaches the claimed invention as disclosed related to claim 1 above. He also teaches that each of the functional blocks is isolated for test by scan path wrappers. He thus teaches an SOC having at least one functional block, controlled by a block clock and at least one scan chain. He also teaches (col. 2, lines 59-62) that a specific scan chain may be selected by chain selector which is controlled by test access port. He thus teaches limitations pertain to debug trigger signal, selecting from the at least one scan chain containing at

least one register element. He further teaches (col. 3, lines 5-7) a control signal TMS gates input signal through multiplexer, a test clock TCK that shifts the inputs present at serial input line and outputs are shifted out serial output line TDO. He thus teaches providing control of the selected scan chain, shifting out the contents of the at least one register element in the selected scan chain and utilizing contents to debug the SOC.

11. As per claim 9, With reference to recognizing a debug ack signal inputted by a user. Moberly teaches (col. 3, lines 5-7, lines 59-61).

12. As per claim 10, With reference to identify a subsequent scan chain, repeating the configuring, providing, shifting and utilizing steps. Moberly teaches (col. 4, lines 13-17).

13. As per claim 11, With reference to recognizing the deactivation of the debug signal and returning each block clock to its operative state. Moberly teaches (col. 3, lines 12-15).

14. As per claim 12, With reference to configuring each of the at least one register elements in the selected scan chain with test values. Moberly teaches (col. 4, lines 1-5).

15. As per claim 13, With reference to disabling all clocks to the cells containing nonscan flip-flops and disabling all clocks to the cells while the debug trigger signal is active. Moberly teaches (col. 3, lines 18-20).

16. As per claim 14, With reference to controlling a bidirectional data bus, and disabling the devices while the debug trigger signal is active. Moberly teaches (col. 3, lines 17-20, 40-43).

17. As per claim 15 With reference to means for utilizing comprises a computer. Moberly teaches (col. 3, lines 59-62).

18. As per claim 16, With reference to the computer is at a location remote from the SOC. Moberly teaches (col. 3, lines 66-67).

19. As per claim 17, With reference to the computer comprises means for automatically debugging the SOC. Moberly teaches (col. 3, lines 40-44).

20. As per claim 18, With reference to means for running a software model of the SOC, and means for comparing the expected system contents values. Moberly teaches (col. 4, lines 1-5, col. 3, lines 46-48).

21. As per claim 19, Moberly substantially teaches the claimed invention as disclosed related to claim 8 above. He also teaches that each of the functional blocks is isolated for test by scan path wrappers. He thus teaches an SOC having at least one functional block, controlled by a block clock and at least one scan chain. He also teaches (col. 2, lines 59-62) that a specific scan chain may be selected by chain selector which is controlled by test access port. He thus teaches limitations pertain to debug trigger signal, selecting from the at least one scan chain containing at least one register element. He further teaches (col. 3, lines 5-7) a control signal TMS gates input signal through multiplexer, a test clock TCK that shifts the inputs present at serial input line and outputs are shifted out serial output line TDO. He thus teaches providing control of the selected scan chain, shifting out the contents of the at least one register element in the selected scan chain and utilizing contents to debug the SOC.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI